In the Claims:

Claim 1 (currently amended): A method of forming an integrated circuit comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate;

forming a an ultra-uniform silicide on the source/drain junctions and on the gate within a thermal budget having a temperature dependent upon a silicide metal;

depositing an interlayer dielectric having contact holes therein above the semiconductor substrate;

forming contact liners in the contact holes within the thermal budget for forming the ultra-uniform silicide; and

forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

Claim 2 (previously presented): The method as claimed in claim 1 wherein:

forming the contact liners uses an atomic layer deposition process.

Claim 3 (canceled)

Claim 4 (currently amended): The method as claimed in claim 1 wherein:

forming the ultra-uniform silicide forms ~~a~~ an ultra-uniform nickel silicide.

Claim 5 (original): The method as claimed in claim 1 wherein:

forming the contacts forms a tungsten material; and

forming the contact liners forms a tungsten nitride material.

Claim 6 (currently amended): A method of forming an integrated circuit comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate;

forming a ultra-uniform nickel silicide on the source/drain junctions and on the gate within a thermal budget having a temperature of less than about 400 degrees centigrade, the ultra-uniform nickel silicide being formed by using a very low power vapor deposition process;

depositing an interlayer dielectric having contact holes therein above the semiconductor substrate;

forming tungsten nitride contact liners in the contact holes within the thermal budget for forming the ultra-uniform nickel silicide; and

forming tungsten contacts in the contact holes over the contact liners.

Claim 7 (original): The method as claimed in claim 6 wherein:

forming the tungsten nitride contact liners uses an atomic layer deposition process.

Claim 8 (canceled)

Claim 9 (currently amended): The method as claimed in claim 6 wherein:

forming the ultra-uniform nickel silicide uses ~~an ultra-thin thickness of~~ a nickel silicide metal having a thickness of not more than 50 Angstroms.

Claim 10 (original): The method as claimed in claim 6 wherein:

depositing the interlayer dielectric deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

Claim 11 (currently amended): An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

source/drain junctions in the semiconductor substrate;

an ultra-uniform ~~ultra-thin~~ silicide on the source/drain junctions and on the gate;

an interlayer dielectric having contact holes therein above the semiconductor substrate;

contact liners in the contact holes; and

contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

Claim 12 (currently amended): The integrated circuit as claimed in claim 11 wherein:

the ultra-uniform silicide is ~~a~~ an ultra-uniform nickel silicide.

Claim 13 (canceled)

Claim 14 (original): The integrated circuit as claimed in claim 11 wherein:

the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

Claim 15 (original): The integrated circuit as claimed in claim 11 wherein:

the contacts in the contact holes are materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

Claim 16 (original): The integrated circuit as claimed in claim 11 wherein:

the contacts are a tungsten material; and

the contact liners are a tungsten nitride material.

Claim 17 (currently amended): An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

source/drain junctions in the semiconductor substrate;

an ~~ultra-thin thickness of a~~ ultra-uniform nickel silicide on the source/drain junctions and on the gate,

an interlayer dielectric having contact holes therein above the semiconductor substrate;

tungsten nitride contact liners in the contact holes; and

tungsten contacts in the contact holes over the contact liners.

Claim 18 (canceled)

Claim 19 (original): The integrated circuit as claimed in claim 17 wherein:

the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

Claim 20 (original): The integrated circuit as claimed in claim 17 wherein: the nickel silicide further comprises arsenic doping.